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EXAMINER	
WOLDEGEORGIS, ERMIAS T	

ART UNIT	PAPER NUMBER
2893	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,828	SUZUKI ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8 and 15-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Foreign Document*.

DETAILED ACTION

1. ***Response to Amendment***

Claims 3-6 and 9-14 have been cancelled; claims 1-2 have been amended; claims 15-25 have been newly added; and claims 1-2, 7-8 and 15-25 are currently pending.

2. ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

3. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilg et al. **(USPN 6130145, hereinafter "Ilg")** in view of

In regards to claim 1, Ilg discloses (Figs. 2A-2C) a semiconductor device comprising: a semiconductor substrate **(201)**; a gate insulator **(220)** formed on the substrate **(201)**; and a gate electrode **(240)** having a metallic compound film **(col. 4 lines 32-36)** , the gate electrode **(240)** being formed on the insulator **(220)**, wherein: the metallic compound film **(WSi_x, col. 4 line 61)**

contains the metal **(W)** in the metal carbonyl **($W(CO)_6$, col. 4 line 65)** and at least one of Si and N **(Si, col. 4 line 60-62).**

Ilg fails to explicitly teach the content of at least one of Si and N in the metallic compound film is such that the work function of the metallic compound film is in the mid-gap of Si.

Lee **(USPN 5164805, hereinafter "Lee")** while disclosing complementary field effect transistor (abstract) teaches the content of at least one of Si and N in the metallic compound film is such that the work function of the metallic compound film is in the mid-gap of Si **(the material of the gate electrode has a work function which places its Fermi level close to the middle of the silicon band gap ... the gate material is ... tungsten silicide (4.7ev), col. 3 line 64 through col. 4 line 16).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Si in the metallic compound film such that the work function of the metallic compound film is in the mid-gap of Si because as taught by Lee in col. 3 line 64 through col. 4 line 16, having a gate material with a work function mid-gap of Si would result in a desirable threshold voltage for the sub-micrometer devices.

In regards to claim 2, Ilg discloses the metal ~~constituting the metal carbonyl~~ is selected from the group consisting of W, Ni, Co, Ru, Mo, Re, Ta, and Ti **(col. 4 lines 30-36).**

In regards to claim 7, Ilg discloses the metallic compound film is doped with an n-type impurity or a p-type impurity **(col. 4 lines 35-38)**.

In regards to claim 15, Ilg as modified by Lee discloses **(col. 4 lines 18-30, Lee)** the metallic compound film **(WSi, col. 4 lines 13-15)** used for a gate electrode of PMOS or NMOS of a MOS device

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ilg in view of Lee as applied to claim 1 above, and further in view of Komatsu **(JP 10303412 , hereinafter "Komatsu")**.

In regards to claim 8, Ilg as modified above discloses all limitations of claim 1 but fails to explicitly teach the gate electrode **(11)** further comprises a silicon film **(14)** formed on the metallic compound film **(13)**

Komatsu discloses (Fig. 3) the gate electrode **(11)** further comprises a silicon film **(14)** formed on the metallic compound film **(13).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ilg by Komatsu because as taught by Komatsu in Par [0023], having a poly-silicon film on WSi_x would help reduce the internal stress generated by the

tungsten silicide film while keeping the gate electrode thick enough to block ion implantation into the channel.

6. Claims 16-20, 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilg in view of Matsuo et al. **(US 2003/0143825 A1, hereinafter "Matsuo")**.

In regards to claim 16, Ilg discloses (Figs. 2A-2C) a method for manufacturing a semiconductor device including a gate electrode **(240)** having a metallic compound film **(col. 4 lines 32-36)**, the method comprising:
preparing a material containing a metal carbonyl **(col. 4 lines 64-65)**, and at least one of a Si-containing material and a N-containing material **(col. 4 line 61-63)**; and
forming, by CVD using the prepared materials **(col. 5 lines 1-7)**, the metallic compound **(WSi, col. 4 line 60-61)** film containing a metal **(W precursors include ... col. 4 lines 63-65)** in the metal carbonyl **(W[CO]$_6$, col. 4 line 65)** and at least one of Si and N **(Si precursors include ... col. 4 lines 61-63)**.

Ilg fails to explicitly teach that by controlling film deposition conditions, the content of at least one of Si and N in the metallic compound film is adjusted such that the work function of the metallic compound film is in the mid-gap of Si.

Matsuo while disclosing a semiconductor device (abstract) teaches **(Fig. 2)** by controlling film deposition conditions, the content of at least one of Si and N in the metallic compound film is

adjusted such that the work function of the metallic compound film is in the mid-gap of Si **(see also Par [0041]).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ilg by the method and/or concept of Matsuo because as taught by Matsuo in Par [0043], it would be possible to make the threshold voltage of each of the n-type MISFET and P-type MISFET appropriate by optimizing the work function of the gate electrode included in each of the n-type MISFET and p-type MISFET.

In regards to claim 17, Ilg discloses the metal constituting the metal carbonyl is selected from the group consisting of W, Ni, Co, Ru, Mo, Re, Ta, and Ti **(col. 4 lines 60-67).**

In regards to claim18, Ilg discloses the metal carbonyl is $W(CO)_6$ (***col. 4 lines 60-67)*** .

In regards to claim 19, Ilg discloses the Si-containing material is selected from the group consisting of silane, disilane, and dichlorosilane (***col. 4 lines 60-67)***.

In regards to claim 20, Ilg as modified above discloses all limitations of claim 1 but fails to explicitly teach the N-containing material is selected from the group consisting of ammonia and monomethyl hydrazine.

However, it is well known in the art of manufacturing semiconductor device to us NH_3 as a source for nitrogen for the deposition of WSiN layer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use ammonia as a source for nitrogen because it is well known in the art of manufacturing semiconductor device to us NH_3 as a source for nitrogen for the deposition of WSiN layer.

In regards to claim 22, Ilg as modified by Matsuo teaches (Figs. 2A-2C, Ilg) the metallic compound film is doped with an n-type impurity or a p-type impurity **(col. 4 lines 65-66).**

In regards to claim 25, Ilg as modified by Matsuo discloses the metallic compound film is used for a gate electrode **(Par [0042], Matsuo)** of pMOS or nMOS of a MOS device **(Pars [0042]-[0043], Matsuo)**.

7. Claims 21 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilg in view of Matsuo as applied to claim 16 above, and further in view of Komatsu.

In regards to claim 21, Ilg as modified above discloses (Figs. 2A-2C, Ilg)the metallic compound film contains the metal in the metal carbonyl, and at least one of Si and N ***(col. 4 lines 60-67)*** but

fails to explicitly teach the metallic compound film contains the metal in the metal carbonyl, at least one of Si and N, and C.

Komatsu while disclosing a semiconductor device and a manufacturing method for the same (Par [0001]) teaches (Fig. 3) the gate electrode **(13/14/20)** comprises: a metallic compound film **(13)**; a barrier layer **(20)** formed on the metallic compound film **(13)**; and a silicon film **(14)** formed on the barrier layer **(20)**; and the barrier layer **(20)** contains the metal and N **(WN_x, see Fig. 3)**;

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ilg by Komatsu because as taught by Komatsu in Par [0023], having a poly-silicon film on WSi_x would help reduce the internal stress generated by the tungsten silicide film while keeping the gate electrode thick enough to block ion implantation into the channel.

Ilg as modified by Komatsu fails to specifically and/or explicitly teach that the barrier layer contains metal, N and C.

It is well known in the art of manufacturing semiconductor device to interchangeably use WCN and WN_x for the purpose of diffusion barrier.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute the barrier layer, WN_x, by a known barrier layer material,

WCN, because it is well known in the art of manufacturing semiconductor device to interchangeably use WCN and WN_x for the purpose of diffusion barrier. Furthermore, it would have been obvious to one of ordinary skill in the art to replace the prior art barrier layer WN_x with another known barrier layer WCN which is known to serve as a diffusion barrier, because one of ordinary skill in the art would have been able to carry out such a substitution, and the results were reasonably predictable. ***See In re O 'Farrell, 853 F.2d 894, 7 USPQ2d 1673 (Fed. Cir. 1988).***

In regards to claim 23, Ilg as modified by Matsuo discloses all limitations of claim 16 above but fails to explicitly teach forming a silicon film on the metallic compound film.

Komatsu discloses forming a silicon film **(14)** on the metallic compound film **(13).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a silicon film on the metallic compound film because as taught by Komatsu in the abstract and Pars [0014]-[0016], this would help alleviate the superfluous tensile stress to gate oxide by thinning the WSi_X while the entire gate electrode being thick enough by forming polysilicon on WSi. As a result of this, the reliability of the whole integrated circuit would be improved.

In regards to claim 24, Ilg as modified above discloses all limitations of claim 21 above but fails to explicitly teach the C- containing material is selected from the group consisting of ethylene, allyl alcohol, formic acid, and tetrahydrofuran.

However, it is known in the art of manufacturing semiconductor devices ethylene is used as carbon-containing source gas for the incorporation of C into a metal compound film (please see US 2001/0014521, Par [0028]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use ethylene as a carbon-containing source gas for the incorporation of C into metal compound film because it is known in the art of manufacturing semiconductor devices ethylene is used as carbon-containing source gas for the incorporation of C into a metal compound film (please see US 2001/0014521, Par [0028]).

8. ***Response to Arguments***

Applicant's arguments with respect to claims 1 and 16 have been considered but are moot in view of the new ground(s) of rejection.

9. ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 6:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/
Examiner, Art Unit 2893

/A. Sefer/
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